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A New Topology for 7-Level Multilevel Inverter with Different PWM Techniques

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Abstract—*Multi-level inverter has a capability to handled high power high voltage with less total harmonic distortion (THD), reduced switching losses and good power quality due to which in recent year they become more popular in high power high voltage application, with Increase in the voltage level, harmonic content in output voltage waveform will decrease. Multi-level has some disadvantage that their complexity requires greater count of power devices and has complex control circuitry. This paper present a novel multi-level inverter topology using one bidirectional switch with other unidirectional switches and which is implemented in single-phase 7- level voltage level. Simulation result of and 7-level can be obtained by MATLAB/ SIMULINK software multi-level inverter using different PWM technique. This topology has less count of power switches and less complexity as compare to other multi-level inverter. For 7-level multi-level inverter multicarrier PWM technique is used to generate different output.*

Keywords — ***Multi-level inverter (MLIs); OPTIMIZATION and PWM techniques.***

I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975. In recent years, multi-level inverter has drawn a great attention in industry, due to use in high power and high voltage application [1-3]. The word 'multi-level inverter' was first introduced in year 1970s and 1980s [4-6]. Multi-level inverter basically start with three voltage levels [6] that can used in high power medium voltage application due to its advantage over the two levels inverter such as, low switching frequency hence reduction in switching losses, lower harmonic, low common mode voltage. Output voltage of multilevel inverter produces a staircase waveform, in other word multiple step voltage waveform which appears like a sinusoidal waveform. Multilevel inverter has some drawback that by increasing the number of voltage levels, higher numbers of semiconductor switches required with separate gate driver circuit. Due to this it increase the size and complexity of the circuits, different pulse - width modulation (PWM) techniques are used to control [7] the output voltage within multi-level inverter. The conventional multi-level inverters topology can be classified as Diode clamped multilevel inverter (DCMLI) [8, 10], Flying capacitor inverter (FCMLI) [1], cascaded H-bridge multilevel inverter (CHBMLI) [9,12]. Diode clamped multilevel inverter are also called as neutral point clamped multilevel inverter proposed by nabae [6] and they use clamped diode, dc capacitor for the generation of Ac voltage. The flying capacitor inverter uses extra capacitor to clamp the connecting point of semiconductor devices which are connected in series. Cascaded h-bridge multilevel inverter consists of separate dc links for each h-bridge cell so it is easily controllable. Cascaded h-bridge multilevel inverter has some drawback that by increasing the number of voltage levels numbers of switching devices given by 2(N+1) also increase. Where N= number of voltage levels. Due to increase in number of voltage levels circuit become complex, efficiency and reliability may be reduced. This paper present a new multilevel inverter topology using H-bridge which is implemented in single -phase . This paper present 7-level multilevel inverter with different PWM technique which is used for controlling the output voltage within inverter. Multicarrier PWM technique is used to generate different output voltage level for 7-level. This new multilevel inverter topology as less number of switches.

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II. PROPOSED TOPOLOGY

The block diagram of multi-level inverter using optimization topology is shown in Fig. 2.1. In this figure, the right side h-bridge is connected which is used to generates the required positive level is called positive level generator and generate negative level is called negative level generator.

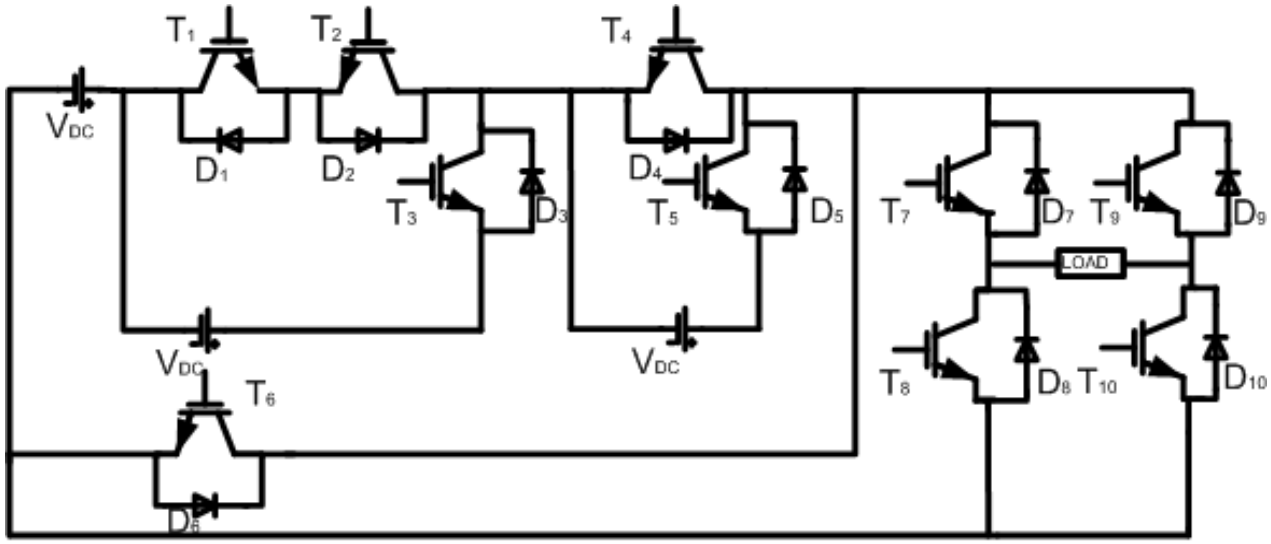

Figure 1: single phase7-Level Multilevel Inverter with Converting Its Optimal Structure

The main purpose of this paper is to control the EMI, minimize the total harmonic distortion with different PWM techniques using Optimization topology and it also minimizes power semiconductor switches than conventional multilevel inverter. For a conventional single-phase 7-level inverter model, it uses 12 switches, whereas the proposed model uses only 9 switches in which one switch is bidirectional [12]. This optimization multilevel inverter easily extends to higher voltage levels by increasing the middle section as shown in Fig. 2.1 fixed dc voltage values. In comparison with a cascade topology, it requires just one-third of isolated power supplies used in a cascade-type inverter. The operation of the proposed topology has been discussed in detail and has been verified with the help of simulations. The proposed topology is a symmetrical topology since all the values of all voltage sources are same.

This MLI topology has been proposed which reduces the overall number of switching devices from conventional MLI topology. They has less count of power devices as compare to cascaded h-bridge MLI as shown in Fig.1. It has three separate dc source as 7-level MLI. The new proposed topology can be easily extended to any required number of voltage levels by increasing the middle part of circuit. This proposed topology is symmetrical topology with all voltage sources have equal value and same to be used for three-phase MLI. The proposed 7-level MLI can operates in different modes which are as given. Operation of the single-phase 7-level MLI with reversing Voltage topology can be easily explained with the help of fig. 1and table 1. When switches T1 T2, T4, T7 and T10 are turned “on” the output voltage will be “Vdc” (i.e., level 1). The output voltage will be “2Vdc” (i.e., level 2) when switches T3, T4, T7 and T10 are turned “on”. When T3, T5, T7 and T10 switches are turned “on” the output voltage will be “3Vdc” (i.e., level 3). When switches T6, T7 and T10 are turned “on” the output voltage is zero (i.e., level 0). Switches T7, T8, T9 and T10 are used for a complementary pair. When T7 and T10 are turned “on” together, positive half cycle (level +1, level +2, level +3) can be generated and when T8 and T9 are turned “on” together, negative half cycle (level -1, level -2, level -3) .The operation of this topology can also be easily understood by mode of operation of single-phase 7-level MLI shown in figure 2. Each voltage source “Vdc” is required 100V. There are seven sufficient switching modes in generating the multistep level for a 7-level MLI.

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TABLE 1: Switching modes of Different Switches Used in 7-level MLI.

Voltage Level	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	Output Voltage
3	Off	Off	On	Off	On	Off	On	Off	Off	On	3Vdc
2	Off	Off	On	On	Off	Off	On	Off	Off	On	2Vdc
1	On	On	Off	On	Off	Off	On	Off	Off	On	Vdc
0	Off	Off	Off	Off	Off	On	On	Off	Off	On	0
-1	On	On	Off	On	Off	Off	Off	Off	On	Off	-Vdc
-2	Off	Off	On	On	Off	Off	Off	On	On	Off	-2vdc
-3	Off	Off	On	Off	On	Off	On	Off	On	Off	-3vdc

III. OPERATING MODE

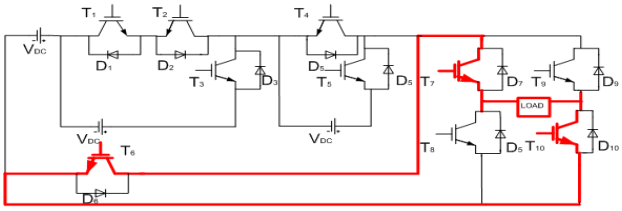

Fig.a : 0 Level , Vo=0v

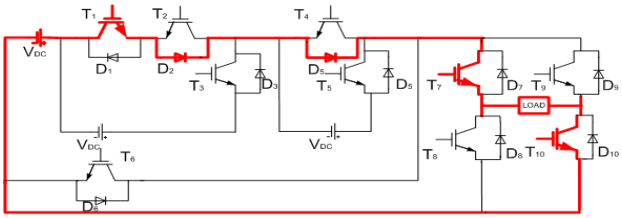

Fig.b : 1 Level , Vo=1v

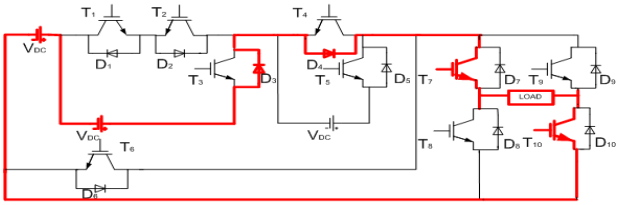

Fig.c : 2 Level , Vo=2v

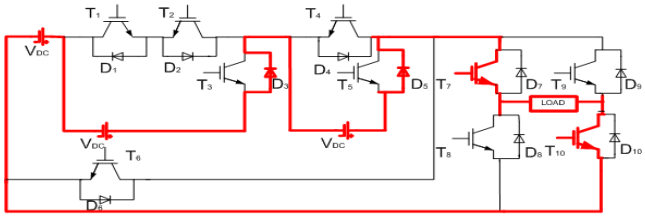

Fig.d : 3 Level , Vo=3v

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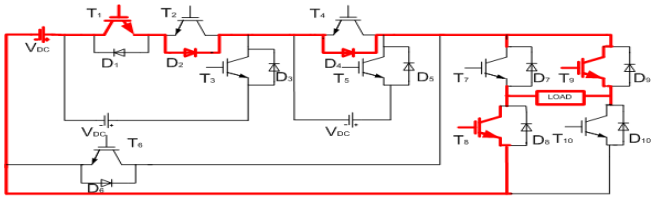

Fig.e : -1 Level , Vo=-1v

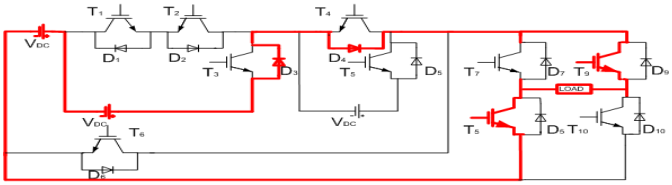

Fig.f : -2 Level , Vo=-2v

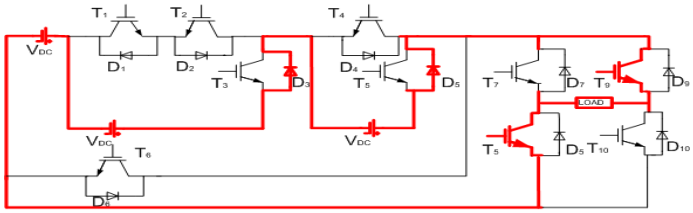

Fig.g : -3 Level , Vo=-3v

Fig.3. Fig (a),Fig (b), Fig (c), Fig (d), Fig (e), Fig (f) and Fig (g) are switching combination of 7-level MLI.

IV. MODULATION STRATEGIES

There are different pulse width modulation strategies with different phase relationships. Phase disposition pulse width modulation (PD PWM):- In phase disposition pulse width modulation strategy, where all carrier waveforms are in same phase shown in fig 3.1 for 5-level MLI For 7-level MLI, 8 triangle carriers are required. For 7-level MLI, 8 triangle carriers are required[1-5].

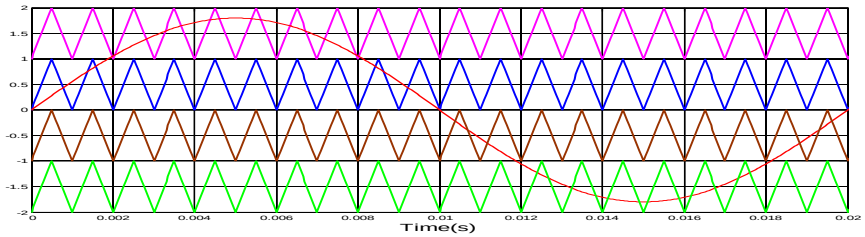

Fig. 3.1: Carrier arrangement for PDPWM strategy (ma=0.9 and mf=20)

- Phase opposition disposition pulse width modulation (POD PWM):- In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are 180^0 out of phase. Shown in fig 3.2[9-11].

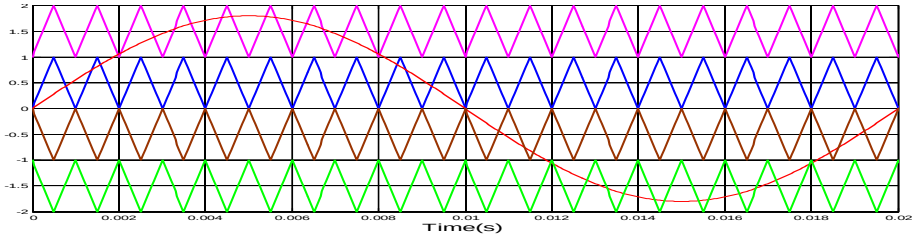

Fig. 3.2: Carrier arrangement for PODPWM strategy (ma=0.9 and mf=20)

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- Alternate phase opposition disposition pulse width modulation (APOD PWM):- In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier by 180^0. Shown in fig 3.3[9-11].

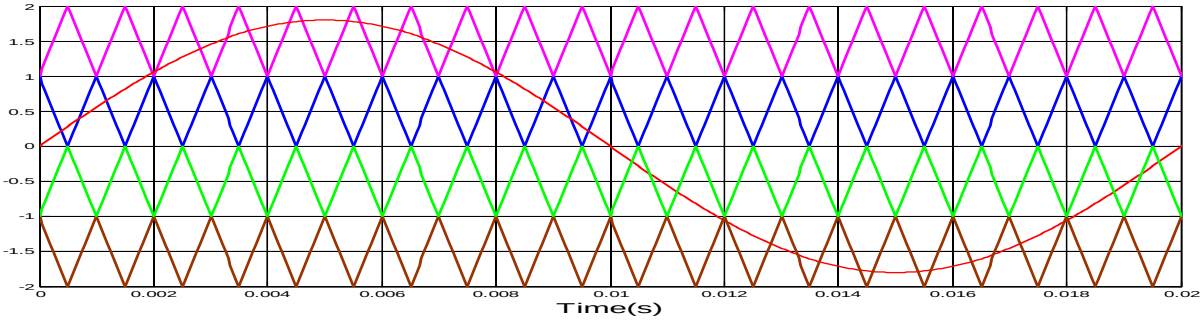

Fig. 3.3: Carrier arrangement for APODP strategy (ma=0.9 and mf=20)

- **Sine Phase Opposition Disposition pulse width modulation (SPOD PWM)**:- Fig.3.4 shows the carrier invert sine wave pulse width modulation strategy. A carrier phase shifted PWM for multi-level inverter is used to generate the stepped multi-level output voltage waveform with lower % THD. Multilevel inverter with N levels requires (N-1) triangular carriers. In phase shifted PWM, all the triangular carriers have same frequency and same peak to peak amplitude.

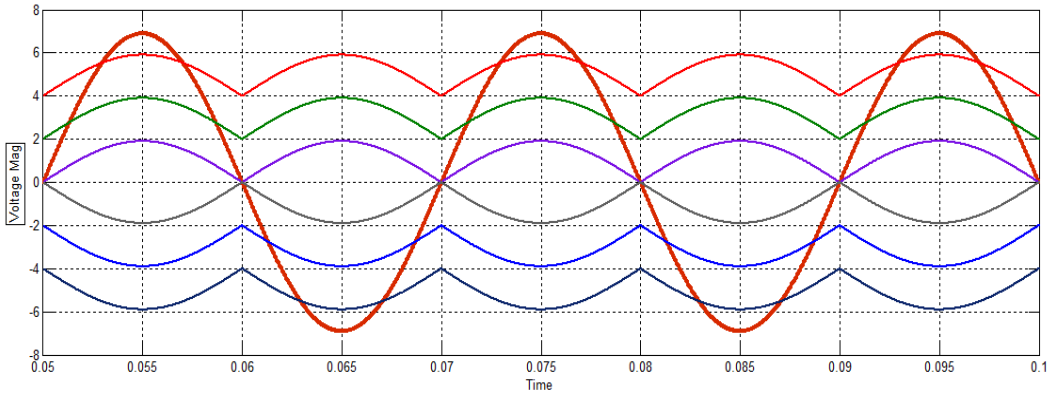

Fig. 3.4: Carrier arrangement for PSPWM strategy (ma=0.9 and mf=20

- **Sine Phase Disposition width modulation (SPD PWM)**):- In invert sine wave pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are in phase. Shown in fig 3.5.

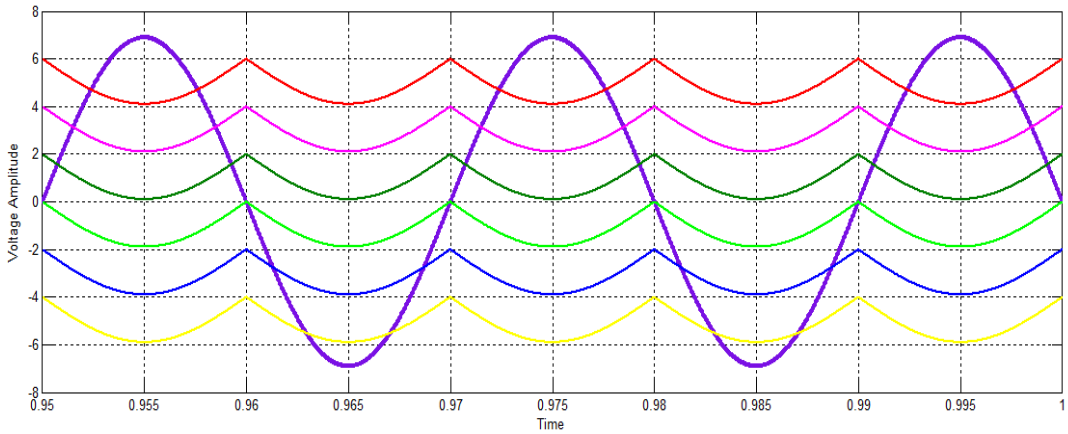

Fig. 3.5: Carrier arrangement for ISPWM strategy (ma=0.9 and mf=20)

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V. OUTPUT WAVEFORM : -

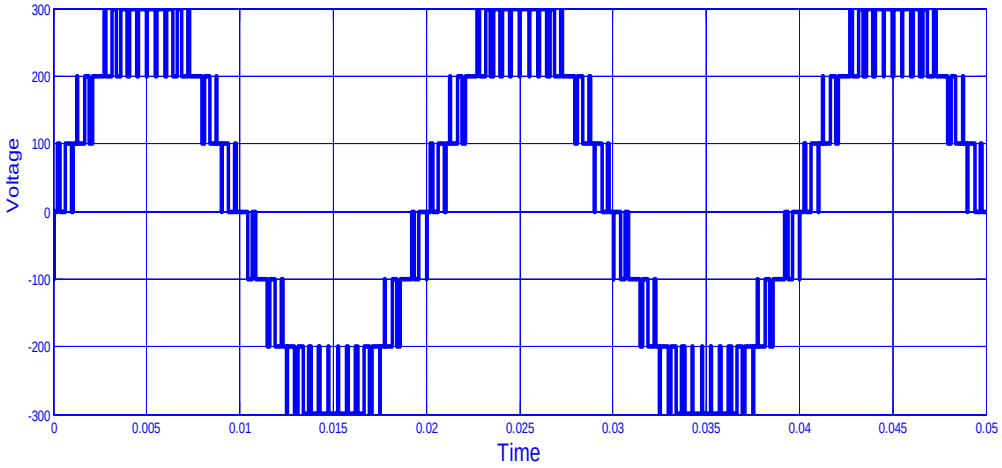

Fig. 5:Output voltage waveform of 7-Level Multilevel Inverter with converting Its Optimal Structure

VI. SIMULATION RESULTS

Table II shows THD comparison between different PWM techniques. The simulation parameters are as following : dc source voltage is 100V; Frequency of carrier signal is 1 kHz. In this paper, four PWM techniques are used PD, POD, APOD, and PS with different modulation index (Ma). For Ma = 0.9, and Mf = 20, corresponding (%) THD are PS = 19.64, PD = 23.61, POD = 23.61, APOD = 19.74,SPD = 14.76 , SPOD = 15.87 shown in Fig. 4.3 – 4.6. Based on the PWM techniques, the harmonic spectrum was analysed using the FFT harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink.

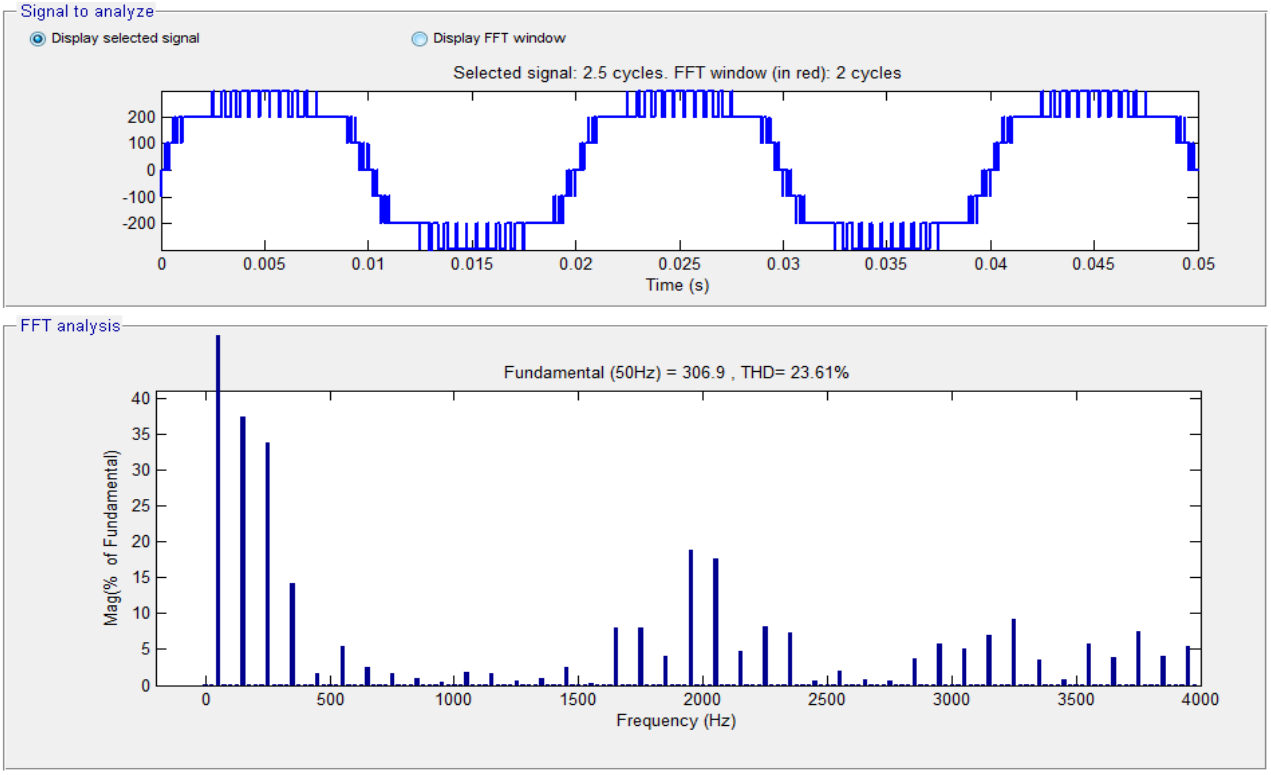

Fig. a: FFT analysis by PDPWM for R-L load (Ma=0.9, Mf=40)

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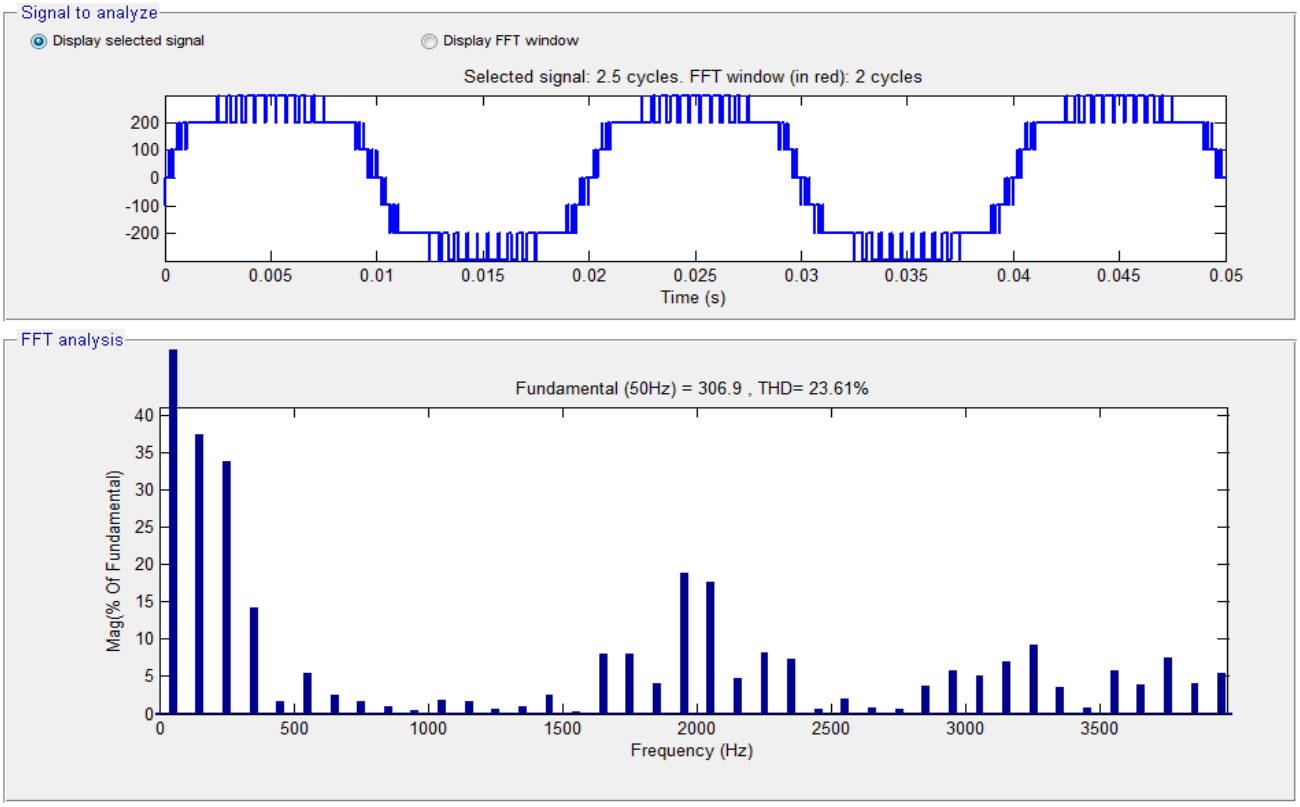

Fig. b: FFT analysis by PODPWM for R- load (Ma=0.9, Mf=40

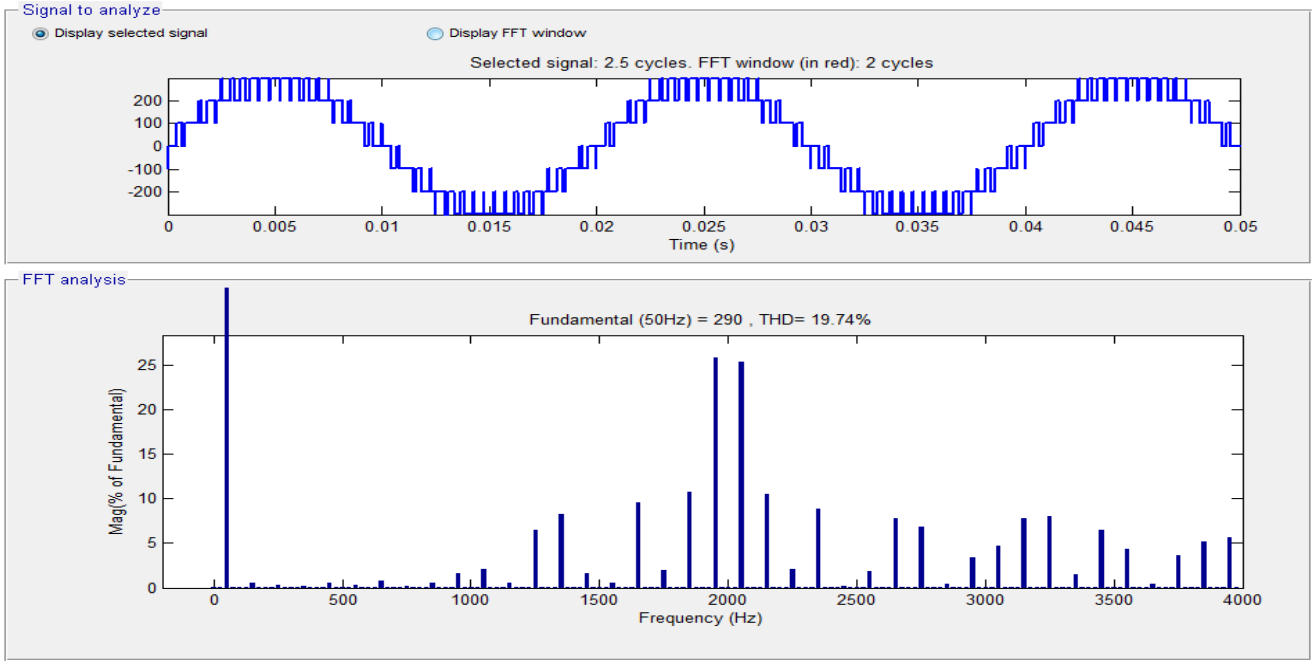

Fig. 8: FFT analysis by APODPWM for R-L load (Ma=0.9, Mf=40).

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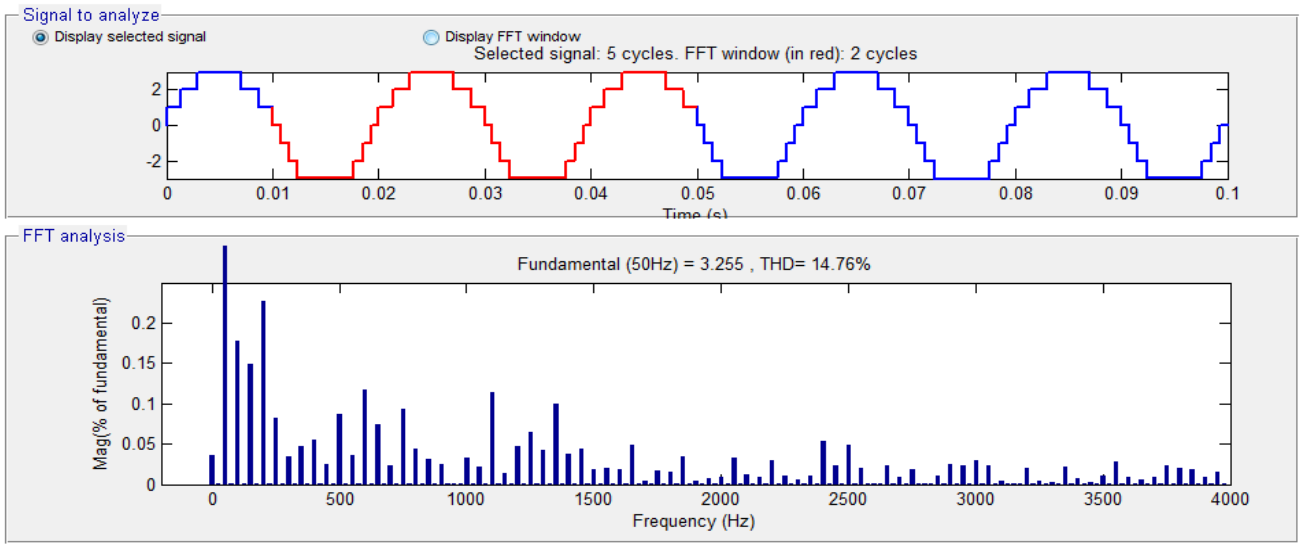

Fig. 9: FFT analysis by SPDWM for R-L load (Ma=0.9, Mf=40).

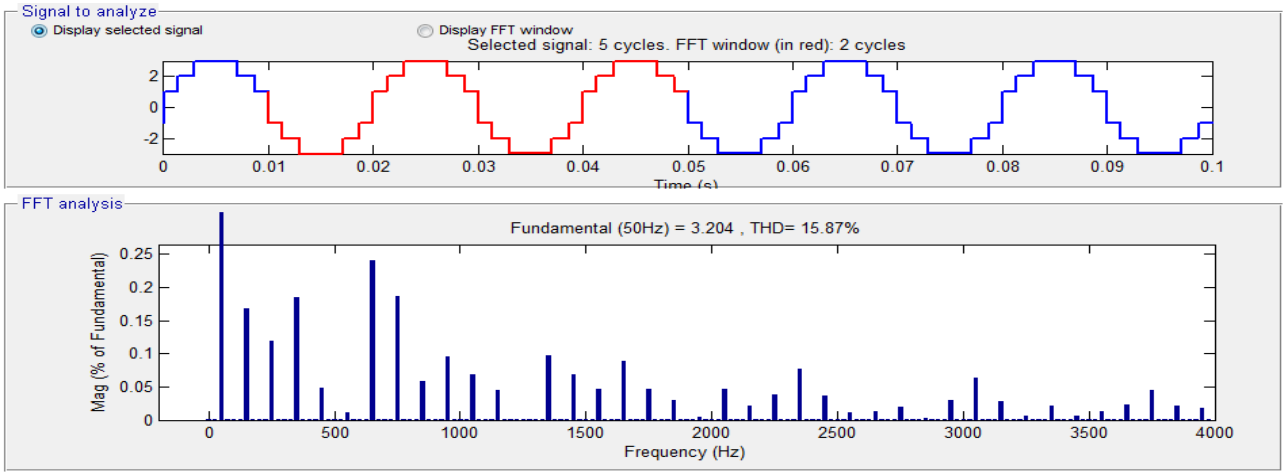

Fig. 10: FFT analysis by SPODWM for R-L load (Ma=0.9, Mf=40).

TABLE-2 Comparison between different multilevel inverter topologies

Modulation Index	PD %THD	POD %THD	APOD %THD	SPD %THD	SPOD %THD
0.933	21.36	21.10	20.93	14.76	15.87
0.966	20.04	19.740	19.746	14.71	15.21
0.990	18.672	18.44	18.54	14.92	14.82
1.000	18.24	18.14	18.36	13.02	13.59

TABLE-3 Comparison between different multilevel inverter topologies

Inverter Topologies	CHB	NPC	Flying capacitor	Proposed Topology
Power Switches	12	12	12	9
Main diode	0	0	0	0
Clamping Diode	0	30	0	0
DC bus Capacitor	0	6	6	0
Flying Capacitor	0	0	15	0
DC source	3	1	1	3

VII. CONCLUSION

In this paper, a 7-level multi-level inverter using optimal topology is proposed with different PWM techniques and proposed MLI topology with different PWM techniques is used to generate 7-level output phase voltage .This topology has been discussed with presented topology. It is proved that the proposed work of Single phase 7-level MLI output voltage total harmonics distortion is reduced and improve the efficiency of system compare with different conventional topologies of single phase 7-level MLI.Table-3 shows the number of power switches [IGBTs] and output voltage steps in the proposed topology. This proposed MLI topology requires less number of components as compared to conventional MLI inverters.

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