A Study on Switch Fabric Architecture in ATM Networks by using VLSI Method

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INTRODUCTION

VLSI design and implementation of a new cell-based high-speed multicast switch fabric using the 0.18 mum CMOS technology. Using distributed control, multistage interconnection network structure, and modular design, the multicast balanced gamma (BG) switch features a scalable, high performance architecture for unicast, multicast and combined traffic under both uniform and non-uniform traffic conditions. The BG switch follows predominantly an output-buffered architecture and utilizes a self-replication mechanism for multicast traffic switching. We are developing ATLAS I, a single-chip ATM switch with optional credit-based (backpressure) flow control. The chip has 16 input and 16 output serial gigabaud pins, and can be configured as a 16 x 16 switch at 622 Mb/s/link, or a 4 x 4 switch at 2.5 Gb/s/link, or in various combinations thereof. It offers sub-microsecond cut-through latency, multicasting, three priority levels (service classes), a 256-cell on-chip shared buffer that contains multiple logical queues organized per-output and per-priority, on-chip VP/VC translation table (4096 entries), and load monitoring support. ATLAS I is a general-purpose building block for high-speed communication in wide (WAN), local (LAN), and system (SAN) area networking, supporting a mixture of services from real-time, guaranteed quality-of-service to best-effort and bursty and flooding traffic, in a range of applications from telecom to multimedia and multiprocessor networks of workstations (NOW).

The chip can be optionally configured to implement credit-based flow control (multi-lane back-pressure), in hardware, at the individual cell level, at the granularity of 4096 flow groups per link. Network systems can take advantage of this feature in either or both of the following ways. A large switch “box” can be built, with hundreds or thousands of ports, using a switching fabric made of ATLAS I chips, where multi-lane back-pressure is used inside the box to provide the high performance of output queuing at the low cost of input queuing; any desired flow control method can be employed outside the box. Networks that employee credit-based flow control can be built directly out of ATLAS I chips. In SAN or LAN environments, the low latency and the multi-lane back-pressure of ATLAS I provide ATM networking with the features and performance of wormhole routing. This is an ideal setting for making NOW that provide multi-processor performance at affordable cost.

ATLAS I provides hardware support for the accelerated measurement of the cell loss probability (CLP) of the real traffic that passes through the switch. The accelerated measurement algorithm allows real-time monitoring and decision making, even in cases where the CLP is so low that normal measurement methods would be inappropriate for real-time operation due to the required long measurement time.

This 4-million-transistor 0.35-micron CMOS chip is being designed at the Foundation for Research and Technology, Hellas (FORTH), in Heraklion, Crete, Greece, and will be fabricated in 1998 by SGS-Thomson, France; development is within the ASICCOM project of the European Union ACTS Programme.

LITERATURE REVIEW

Coppo et al. (1999) proposed a methodology for evaluation and optimization of Clks networks, used as ATM switching fabrics, based on component count and interconnection cost as physical cost requirements for a given connection blocking probability. Zegura presented a comparison of different switching fabrics based on the count of pin-limited chips needed by each fabric.
Shi et al. (2003) explored the optimization of the Knockout switch hardware cost given certain constraints on the quality of service. Most recently, Schultz studied the performance limits of shared memory architectures using experimental results and technology trend curves. Moreover, almost all of those studies used certain traffic profiles or a certain set of given quality of service parameters that would make the analysis of the physical requirements simpler and more tractable.

**NOTEWORTHY CONTRIBUTIONS**

Bogliolo and Benini et al (2006) proposed another model, the RB model, that is characterization-free for the dynamic power but then uses gate-level simulations to characterize the delay-sensitive second-order power contributions using a regression model. In effect, this is merely modeling the error of the characterization-free part and not necessarily the glitches or short-circuit power. A simpler approach would be to use regression for the whole model. It also assumes that the dynamic power of a certain node is proportional to the transition activity derived from the module Boolean expressions with the node capacitance as the proportionality constant. However, the assumption of the capacitance being independent of the input streams is not always true. For example, the capacitance seen at the inputs of a complex gate differs with the input pattern depending on which transistors are on. The model, however, illustrates other important facts. It shows that not all of the internal node capacitances need to be considered. These node capacitances can be sampled to speed up the characterization with only minor loss of accuracy. It also shows that a uniform random sampling gives the best results. This technique will be used to modify the DBT model as will be described below. Moreover, all of these schemes still need to be generalized to accommodate different types of data representation such as that for network traffic streams commonly found at the input ports of the switching fabrics.

Channamallikarjuna Mattihalli et al (2002) attempt to give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Attempt to provide a multipurpose networking router by means of Verilog code, thus we can maintain the same switching speed with more security as we embed the packet storage buffer on chip and generate the code as a self-independent VLSI Based router. The approach will result in increased switching speed of routing per packet for both current trend protocols, which we believe would result in considerable enhancement in networking systems.

Feng Liang et al (2004) proposed a novel test pattern generator (TPG) for built-in self-test. His method generates multiple single input change (MSIC) vectors in a pattern, i.e., each vector applied to a scan chain is an SIC vector. A reconfigurable Johnson counter and a scalable SIC counter are developed to generate a class of minimum transition sequences. The proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes. Results show that the produced MSIC sequences have the favorable features of uniform distribution and low input transition density.

James Aweya et al (2008) give attention to new powerful architectures for routers in order to play that demanding role. In this work, he identified important trends in router design and outlines some design issues facing the next generation of routers. It is also observed that the achievement of high throughput IP routers is possible if the critical tasks are identified and special purpose modules are properly tailored to perform them.

M. Sowmya et al (2001) he attempt is to give a onetime networking solution by the means of merging the VLSI field with the networking field as now a days the router is the key player in networking domain so the focus remains on that itself to get a good control over the network. This paper is based on the hardware coding which will give a great impact on the latency issue as the hardware itself will be designed according to the need.

**RESEARCH METHODOLOGY**

Research Methodology is a way to systematically solve the research problem, it not only takes the research methods but also consider the logic behind the methods. The study of Research Methodology for developing the project gives us the necessary training in gathering materials and arranging them, participation in the field
work when required, and also provides training in techniques for the collection of data appropriate to particular problems.

**Research Design**

**Exploratory Study**

- **Depth Interview:** It refers that a specific type of qualitative marketing research method whereby data is received from a small group in hopes of determining the motivation for consumer purchasing decisions made.

- **Secondary Data:** Secondary data is the data that have been already collected by and readily available from other sources. Such data are cheaper and more quickly obtainable than the primary data and also may be available when primary data cannot be obtained at all.

**Descriptive Study**

**Cross-sectional Study:** Cross-sectional research is a research method often used in developmental psychology, but also utilized in many other areas including social science and education. This type of study utilizes different groups of people who differ in the variable of interest, but share other characteristics such as socioeconomic status, educational background, and ethnicity.

**EXPECTED OUTCOMES OF THE STUDY**

The expected outcomes of the study will be show how to efficiently scale packet switches to very large numbers of ports, while maintaining non-blocking operation and high quality of service. This will be done by extending the known per-flow backpressure architecture so as to make it applicable to the Benes fabric with multipath routing and cell resequencing. To the best of our knowledge, this is the first time that this combination of architectures is going to study.

**REFERENCES**


