
High Current Gain Multilevel Inverter Using Linear Transformer

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ABSTRACT

Multilevel converters have gained importance because of their ability to generate high quality output waveforms with a low switching frequency and due to multilevel the concept of harmonics distortion decreases in output wave forms. In this paper a new topology is proposed for multilevel inverter using a linear transformer to give a high output Current. The proposed topology is based on using linear transformer. As a result of using inductors, there is a boost in output current, while the currents through the power electronic switches are less. This is not the case in the most of the existing topologies. This structure can be considered as the perfect solution to reduce the nominal values of switches and increase the output current and using linear transformer will completely avoid the voltage balancing problem that occurs in other conventional multilevel inverter. A simulation result of the proposed topology in single-phase scheme using the Mat lab software is presented.

Keywords: multilevel inverter, linear transformer, pulse width modulation control, simulink

I. INTRODUCTION

Recently multilevel converters have gained importance. Many structures and applications have been presented for these converters which are widely applied as the interface of renewable energy sources, power conditioners in power systems and in traction applications. The new structures that have been presented offers different features such as optimizing the structures in terms of components count and size, improving output waveform quality, and reducing losses. There are three well-known topologies for multilevel inverters which include the cascaded H-bridge (CHB), neutral point-clamped (NPC) or diode-clamped, and the flying capacitor (FC) multilevel inverters.

The diode-clamped multilevel inverter requires a large number of clamping diodes and capacitors to generate different voltage levels, and also needs complicated controls for voltage balancing of the dc-link capacitors. Although the three-level diode-clamped inverter has been widely used in industry, it is difficult to extend it to high number of voltage levels. In the Flying capacitor multilevel inverters the voltage of the switches is limited by flying capacitors. The flying capacitor multilevel inverter, unlike the diode-clamped topology, has natural balancing capability due to offering redundant switching combinations. However, the flying capacitor multilevel inverter has the problem of using high number of flying capacitors which results in increasing the size of system.

The cascaded H-bridge multilevel inverters use several H-bridges supplied by the independent dc voltage sources. Based on the value of the dc voltage sources, they can be symmetric or asymmetric. In the symmetric cascaded H-bridge multilevel inverters, all of the dc voltage sources have the same value resulting in a modular topology but using high number of components. In the asymmetric topologies, the dc voltage sources have different values so that more number of voltage levels is generated in comparison with the symmetric topology. However, in the case of asymmetric multilevel inverters the power switches with different voltage ratings are required losing the modularity. In the most of the presented topologies for multilevel inverters, the voltage is shared between the switches but the currents through all of

the switches are equal which is also equal to the load current.

II. PROPOSED SYSTEM

New multilevel inverter topologies have been developed by the use of linear transformer to increase output current. In this way, along with the increase of output current, the current ratings of the power electronic components can be reduced. Using this method, the sizes of inverter's passive elements (inductors and capacitors) are reduced. In addition, the harmonic content of the output voltage is considerably reduced in comparison with the conventional inverters. In this paper, a basic structure is proposed for 5 –level inverters with the ability of increasing output current by power electronic switches with less nominal currents in comparison with the load current. This structure needs fewer elements than those of conventional inverters.

The proposed 5 -level inverter has been simulated in the MATLAB environment to verify its operation. The dc link voltage is considered to be 200V. The inverter supplies an inductive load with the resistance and inductance of 10 ohm and 1mH, respectively. The self-inductance of the coupled inductor windings are the same and equal to 1mH and the mutual inductance is 0.9mH. The fundamental frequency and the switching frequency are 50Hz and 8 kHz, respectively.

Figure 1.Shows the block diagram of the proposed single phase five level inverter with a linear transformer. It uses a PWM controlling method. It includes a driver circuit and a pic microcontroller.

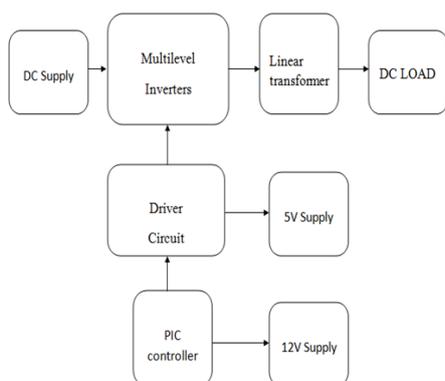


Fig 1: Block diagram of a proposed system

In this paper, a new 5 -level linear transformer based inverter suitable for high-current applications are proposed. The structure of the proposed single-phase inverter includes of a dc voltage source of 200v and 6 power electronic switches (MOSFETs) and a linear transformer of windings 1mH and mutual inductance of 0.9mH.

This topology can be developed to n-phase systems. the proposed inverter is developed for single-phase. For specific current ratings of the switches, the proposed inverter is able to increase the output current and this property can be considered as its main feature. In comparison with the other multilevel inverter, the proposed inverter has less number of switches. Moreover, the proposed topology does not need to split capacitors which avoid voltage balancing problem.

The proposed 5 -level inverter is illustrated in Fig 2. The structure of the proposed inverter is such that it provides 5 - level voltage by using a dc voltage source, the switches S1 to S6 and two inductors connected in series forming a linear transformer at the output. The proposed circuit consists of an H-bridge with two inductors and extra switch leg.

For five levels multilevel inverter the circuit diagram is shown in fig (2). It have six switches and a linear transformer which is connected to RL loads

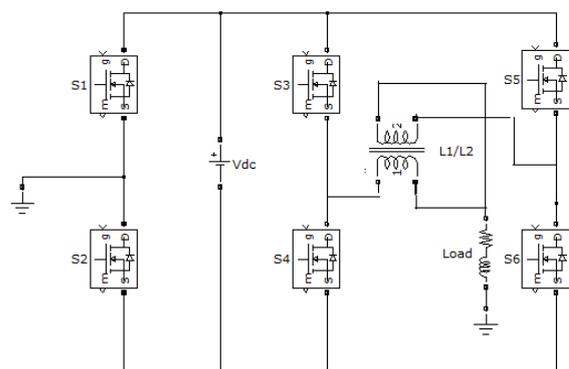


Fig 2: Circuit of single phase 5 level inverter

In this converter, the switches S1 and S2 are switched with fundamental frequency and the current flowing through these switches is equal to output current, whereas, the switches S3 to S6 are switched by switching frequency and their current is half of the output current. In other words, switches with higher current ratings operate in low-frequency and the switches with lower current ratings operate in higher frequency leading to reduction in the

switching stresses. The current reduction in the switches (or output current increase) and generating of five level voltage is achieved by the linear transformer and the appropriate control of switches. The switches S3 and S4 also the switches S5 and S6 are switched complementary.

The pulse width modulation (PWM) control method is used for the proposed converter. Control of the switches S3 to S6 is obtained by comparing the absolute value of reference voltage, with two triangle carrier waves, C_1 and C_2 . These two carrier waveforms have 180° phase shift in reference to each other. For $|V_{ref}| > 0$ the switch S2 is turned on and the switch S1 is turned off. Therefore, the point n, mid-point of switches S1 and S2 is connected to the common point of the switches S4 and S6 which makes the average value of voltages V_{1n} and V_{2n} to be positive. For $V_{ref} < 0$ the switch S1 is turned on and the switch S2 is turned off. In this condition, the point n is connected to the common point of the switches S3 and S5 making the average value of voltages V_{1n} and V_{2n} to be negative.

Considering that the switches S1 and S2 are switching complementary, thus changing the switching mode of these two switches leads to reverse PWM control of the switches S3 to S6 on each half-cycle.

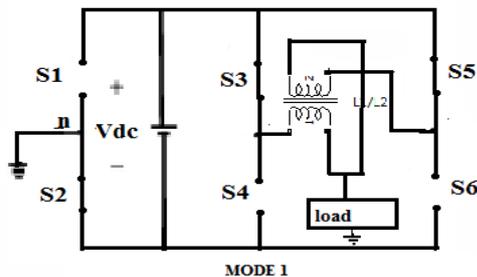
The output voltage of the proposed 5-level inverter includes the voltage levels of $\pm V_{dc} \pm V_{dc}/2$ and 0. Switching modes to generate these voltage levels are given in Table 1.

According to Table 1 there is a particular switching state for each topological mode. The switches S1 and S2 are switching complementary. So, switching modes changing of these switches leads to changes in average values of V_{1n} and V_{2n} . It means that when S1 is turned off and S2 is turned on, V_{1n} and V_{2n} become positive or 0, and when S1 is turned on and S2 is turned off V_{1n} and V_{2n} become negative or 0. Based on this strategy, the different modes of operation take places

Mode 1: when S1 is turned off and S2 is turned on, V_{1n} and V_{2n} become positive or 0, and when S1 is turned on and S2 is turned off V_{1n} and V_{2n} become negative or 0. Based on this strategy, in mode 1, the circuit current is flowed through the coupled inductors by the switches S2 S3 and S5 while the switches S1 S4 and S6 are turned off. So, the source voltage is applied to each of inductors by switches S3 and S5, therefore, the obtained output voltage becomes +Vdc

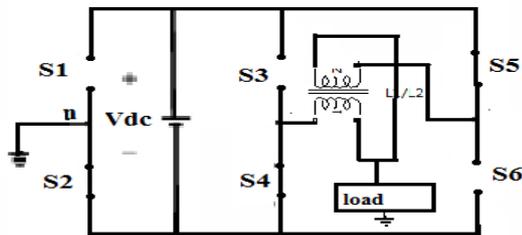
TABLE 1: VARIOUS OPERATING MODES OF A MULTILEVEL INVERTER

Modes	Output Voltage	Inductor Voltages		Switch States					
	V_0	V_{1n}	V_{2n}	S1	S2	S3	S4	S5	S6
1	$+V_{dc}$	V_{dc}	V_{dc}	0	1	1	0	1	0
2	$+V_{dc}/2$	0	V_{dc}	0	1	0	1	1	0
3		V_{dc}	0	0	0	1	1	0	0
4	0	0	0	0	1	0	1	0	1
5		0	0	0	1	0	1	0	1
6	$-V_{dc}/2$	0	$-V_{dc}$	1	0	0	1	1	0
7		$-V_{dc}$	0	0	1	0	1	0	0
8	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	1	0	0	1	0	1



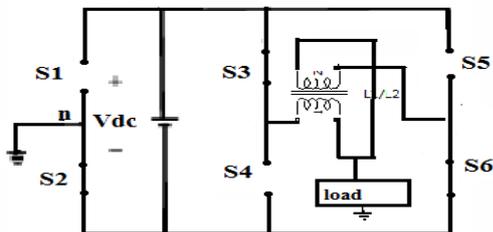
MODE 1

Mode 2: In this mode switch S2 S4 and S5 are turned on and other switches are turned off. The circuit current is flowed by the switches S2 S4 and S5. Thus, V_{1n} is grounded by S4 and the source voltage is applied on V_{2n} . therefore, the obtained output voltage becomes $+Vdc/2$.



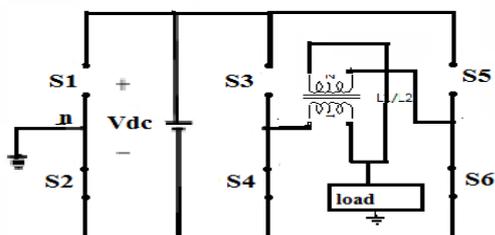
MODE 2

Mode 3: it is observed that the switches S2 S3 and S6 are turned on. And in this mode V_{1n} and V_{2n} are inverted in comparison with mode 2. So, V_{2n} is grounded and V_{1n} is connected to source voltage. Therefore, output voltage is same as mode 2 and equal to $+Vdc/2$.



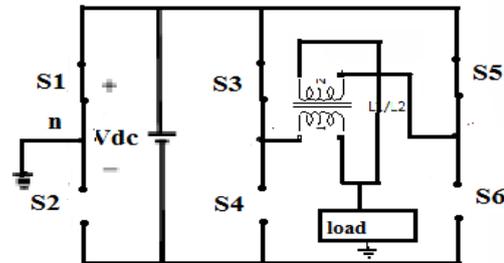
MODE 3

Mode 4: the switches S2 S4 and S6 are turned on, so both V_{1n} and V_{2n} voltages are grounded by switches S4 and S6. As a result, the output voltage of inverter is 0.



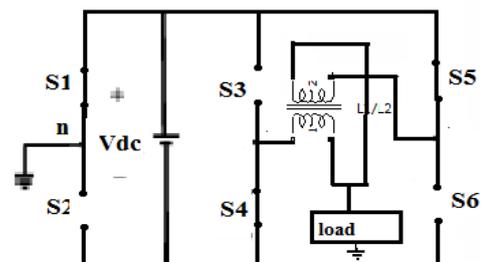
MODE 4

Mode 5: the switches S1 S3 and S5 are turned on and other switches are turned off. The circuit current is flowed through the linear transformer (inductors connected in series) by the switches S1 S3 and S5. The source voltage is applied to each Inductor giving output voltage of $-Vdc$. we observe that mode 5 is a complementary of mode 1.

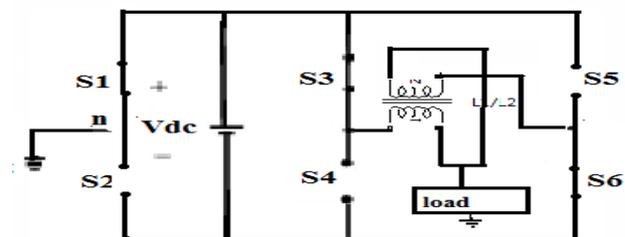


MODE 5

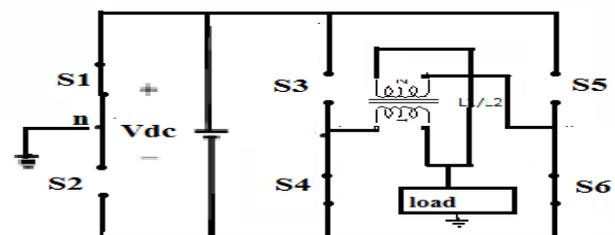
Mode 6: Reverse operation of mode 2 gives us mode 6 operation. In this mode switches S1 S4 and S5 are turned on. So, the current flows through these switches. Giving output voltage of $-Vdc/2$. mode 7 is same as that of mode 6. Which give the same output voltage as that of mode 6 $-Vdc/2$. Mode 8 gives 0 output voltages which are reverse of mode 4 operation.



MODE 6



MODE 7



MODE 8

An important issue in relation to series connected inductors is that the average voltage of transformer windings should be zero to avoid inductors from saturation and to keep inductors currents in normal condition. Thus, regarding this requirement, the following equation should be satisfied continuously:

$$V_o = V_o - V_{2n} \quad [1]$$

Then, the output voltage is:

$$V_o = \frac{v_{1n} + v_{2n}}{2} \quad [2]$$

Also, as the current flowing through the switches S3 to S6 is half of the load current (I_o), the following equation can be written

$$I_{1a} = I_{2a} = I_o/2 \quad [3]$$

Consequently, the inverter output current is equal to the total current flowing in the inductors as follows

$$I_{1a} + i_{2a} = I_o \quad [4]$$

Where I_{1a} and I_{2a} are the currents through each inductor. Some of the benefits of the lower current in inverter's components include the reduction of the switching and conduction losses, reduction of the switches current ratings, and cost reduction as well as output filter reduction.

IV. SIMULATION AND RESULTS

The proposed 5-level inverter has been simulated in the MATLAB environment to verify its operation and shown in fig (4). The dc link voltage is considered to be 200 V. The inverter supplies an inductive load with the resistance and inductance of 10 ohms and 1mH, respectively. The self-inductance of the linear transformer windings are the same and equal to 1m H and the mutual inductance is 0.9mH. the fundamental frequency and the switching frequency are 50 Hz and 8 kHz, respectively.

The simulation results of the proposed single-phase inverter are shown in Fig. 5 to 7. The first trace of the Fig. 5 shows the output voltage of 200v. As the figure shows, all of the expected voltage levels are generated so that the output voltage is a 5-level voltage. The third trace shows the output current 20A in fig 7. The current across

Inductor 10A is shown in second trace of Fig. 6. It is clear that the output current is twice of each inductor's current which indicates the current doubling capability of the proposed topology.

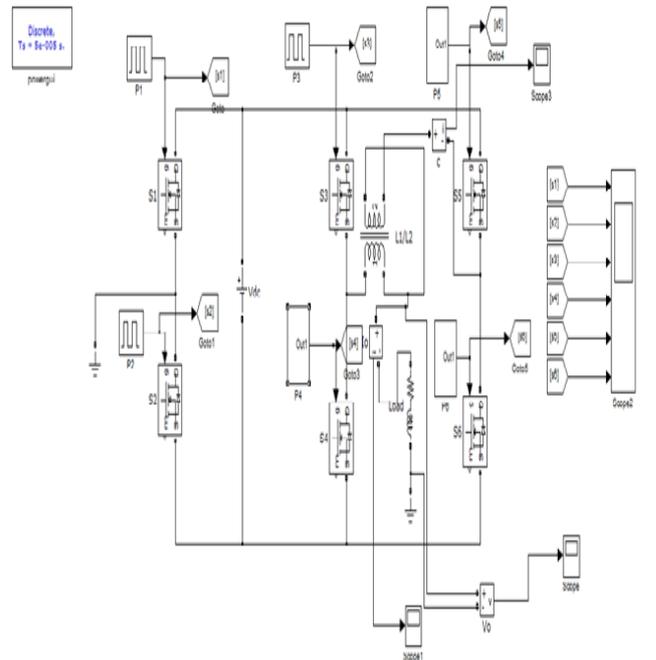


Fig 4: simulation of the proposed system in MATLAB

RESULTS

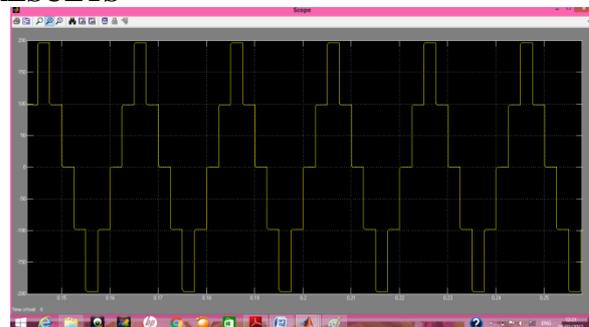


Fig 5: output voltage



Fig 6: current across inductor

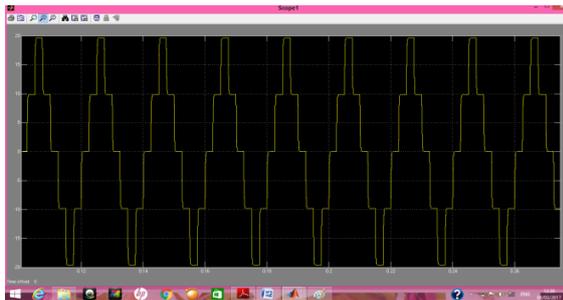


Fig 7: output current

V. CONCLUSION

In this paper a new topology of multilevel inverters with a linear transformer is presented. This modified inverter uses less number of power electronic switches than the conventional multilevel inverter and this modified inverter also avoid voltage balancing problems which occur in the other conventional multi level inverter. For specific current ratings of the switches, the proposed inverter is able to increase the output current which is double of its input current and this property can be considered as its main feature.

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