

# Analysis and Design of a Low Power and Wide Tuning Range Voltage-Controlled Ring Oscillator in 45 nm CMOS Process

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*Abstract --- This Paper reports on design and analysis of CMOS Voltage Controlled Ring Oscillator (VCRO) based on the delay cells proposed by Changzhi Li and Jenshan Lin. The two stage CMOS VCRO exhibits very low power consumption and wide tuning range when realized using GPDK 45 nm CMOS process. The oscillator has a very wide tuning range from 6 GHz to 17 GHz. Because of its wide tuning range, it can be used for electronic warfare applications. It has also very low power consumption of about  $3\mu\text{W}$  with a supply voltage of 1 V. The phase noise of this ring oscillator is found to be  $-78\text{ dBc/Hz}$  @10 MHz offset which can be improved by adding more number of stages.*

*Index Terms --- CMOS, Low Power, Phase Noise, Ring oscillator, Electronic warfare*

## I. INTRODUCTION

Phase Locked Loop (PLL) is used in wide range of communication systems for synchronization and demodulation process. Voltage Controlled Ring Oscillators is one of the key components in a PLL. The wide frequency range of PLL attributes to the tuning range of VCO. Hence VCO with wider and linear tuning range are extensively used in various applications such as radar, electronic warfare, electromagnetic weapons like electromagnetic generators etc.

The design of a high performance CMOS VCO in terms of optimized parameters like Tuning range, power consumption and phase noise has been a challenging task in recent years.

A CMOS VCO can be implemented using LC tuned circuit or ring topology. LC-oscillators [1] exhibits good phase noise performance but it fails in other aspects like firstly, the operating frequency is low

as compared to ring oscillators. Secondly, the chip area is very high due to presence of spiral inductors which leads to high costs. Thirdly, the phase noise performance factor depends on the quality factor of inductors as a result of which the cost of a good quality LC oscillator is high. On contrary, ring oscillators provide much better tuning range and occupy very less chip area for fabrication which is very cost effective. It can generate both in-phase and quadrature outputs for even number of delay cells.

This paper analyzes a two stage CMOS differential ring oscillator proposed by Changzhi Li and Jenshan Lin [2] using 45 nm technology. It is redesigned with varying the design parameters to achieve high tuning range and low power consumption.

The remaining part of the paper is organized as follows. Section II presents the analysis of architecture of delay cell used in this VCO. Section III shows the simulation studies of the tuning range, power consumption and phase noise. In section IV simulation results are compared with other works and eventually in section V provides some conclusions.

## II. CMOS Ring VCO

The ring oscillator consists of two cascaded delay cell connected in differential configuration whose delay is controlled by the control voltage  $V_{\text{CTRL}}$  as shown in figure 1. The differential delay structure provides better substrate common noise rejection as well as lowers the noise injection into the other

circuits in the same substrate and also provides quadrature output for different applications.

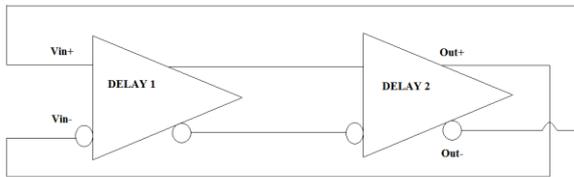


Figure. 1: Building block Diagram of VCRO proposed in [2].

The schematic of each delay cell is shown in figure2. The delay cell includes a PMOS diode pair (Mp1 and Mp4), two PMOS transistors (MP2 and MP3) in cross-coupled manner to provide positive feedback for oscillation. The NMOS transconductance pair (MN1 and MN2) are used to achieve higher frequency of oscillation and one NMOS transistor (MN3) for adjusting the tuning range of VCRO.

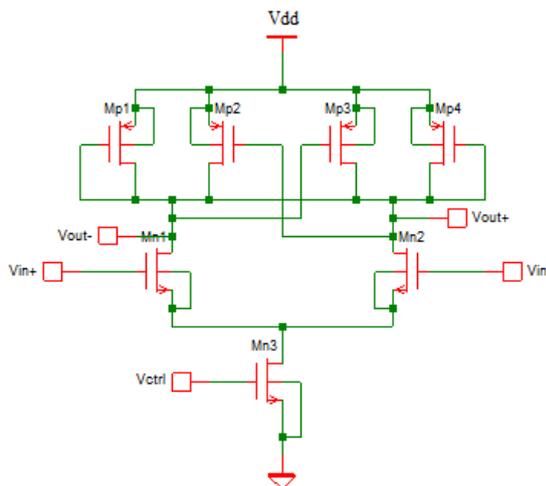


Fig. 2: Schematic of each delay cell

#### A. WIDE TUNING RANGE

The half circuit of the delay cell is analyzed and the loop gain of the oscillator can be expressed as

$$H(s) = \frac{V_o}{V_{in}} = - \left( \frac{g_{mn1}}{(G_{ds} + g_{mp1} - g_{mp2}) + sC_L} \right)^2 \quad (1)$$

where  $G_{ds} = g_{dsn1} + g_{dsp1} + g_{dsp2}$  is the resistive load due to channel-length modulation,  $g_m$  is the transconductance,  $g_d$  is the channel conductance. The total phase shift of the delay cell chain is  $180^\circ$  (each delay cell provides  $90^\circ$  phase shift) and the

overall gain is maintained at unity satisfying the Barkhausen criteria of oscillation. The condition is achieved by making  $(G_{ds} + g_{mp1} - g_{mp2} \ll sC_L)$ .

The oscillation frequency of the proposed ring oscillator is derived as

$$\omega_{osc} = \frac{\sqrt{g_{mn1}^2 - (G_{ds} + g_{mp1} - g_{mp2})^2}}{C_L} \quad (2)$$

By controlling the transconductance ( $g_m$ ) of the diode controlled PMOS devices  $M_{p1}$  and  $M_{p4}$ , the output frequency can be tuned and maximized.

#### B. LOW POWER CONSUMPTION

The NMOS input pair (Mn1 and Mn2) is used to maximize the transconductance to capacitance ratio ( $g_m/C$ ) to achieve high operating frequency with low power dissipation. In order to reduce the  $g_m$  requirement and thus power dissipation, only parasitic capacitors of devices are utilized. Moreover, only two delay cells are included in the oscillator to minimize the power consumption.

#### C. PHASE NOISE PERFORMANCE

Phase noise performance is made better by increasing the carrier power and decreasing the noise power. In this circuit, the PMOS devices (Mp2 and Mp3) are directly connected to the supply voltage  $V_{dd}$ . This maximizes the output amplitude and hence, increases the carrier power which results in decrease of noise power [3].

#### D. LINEAR FREQUENCY TUNING

From the delay cell, DC operation point can be expressed as

$$\begin{aligned} V_{DD} &= V_{gsp} + V_{gsn} + V_{dsMn3} \\ &= \sqrt{\frac{2I}{\mu_p C_{ox} L_p}} + V_{thp} + \sqrt{\frac{2I}{\mu_n C_{ox} L_n}} + V_{thn} + V_{dsMn3} \end{aligned} \quad (3)$$

It should be noted that (3) is valid only when the two delay cells are connected to form a ring oscillator. Otherwise  $V_{gsn}$  needs to be replaced by  $V_{dsn}$ . The transistor Mn3 is operated in such a manner that  $V_{dsMn3}$  has little effect on (3) and it should work in deep triode region. Therefore,  $\sqrt{I}$  is

proportional to  $V_{DD} - V_{thn} - V_{thp}$ . From (2) the oscillation frequency can be approximated as

$$\omega_{osc} = \frac{g_{m1}}{C_L} \propto \sqrt{I} \propto V_{DD} - V_{thn} - V_{thp} \quad (4)$$

the oscillation frequency is linearly tuned to  $V_{DD}$ .

### III. SIMULATION RESULTS

The ring oscillator is simulated in GSDK 45nm CMOS Technology in CADENCE tool in Virtuoso Analog Design Environment. The design parameters of the transistors W/L ratio are taken as 120nm/45nm. The tuning range, phase noise and power consumption is measured using cadence tool and summarized in table I.

#### A. TUNING RANGE

Transient response of this ring oscillator at supply voltage  $V_{dd}$  of 1 V and control voltage  $V_{ctrl}$  at 2.5V is shown in Fig. 3. Then by varying the supply voltage ( $V_{dd}$ ) tuning range is obtained and is shown in Fig. 4. Again, the variation between control voltage  $V_{ctrl}$  at different supply voltage  $V_{dd}$  between frequency is analyzed as shown in Fig. 5.

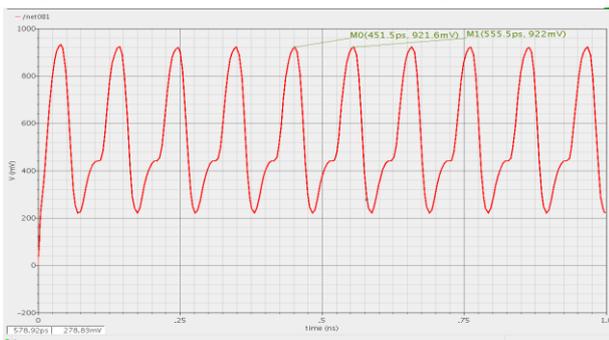


Fig. 3: Transient analysis of VCRO

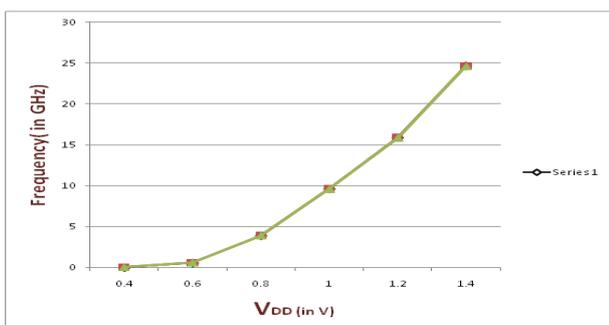


Fig. 4: Simulated Oscillation frequency as a function of VDD

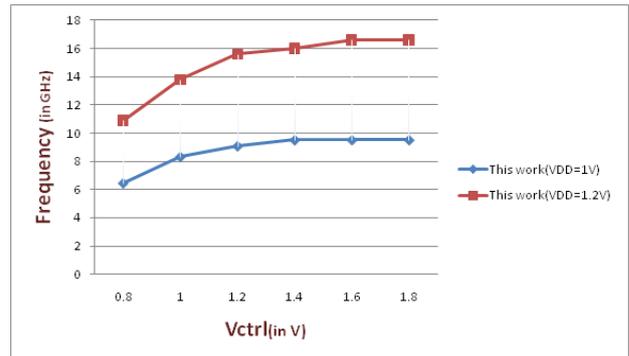


Fig. 5: Simulated Oscillation frequency as a function of Vctrl

#### B. PHASE NOISE

The phase noise of this voltage controlled ring oscillator was found to be about -77.85dBc/Hz at 10MHz offset frequency as shown in Fig. 6.

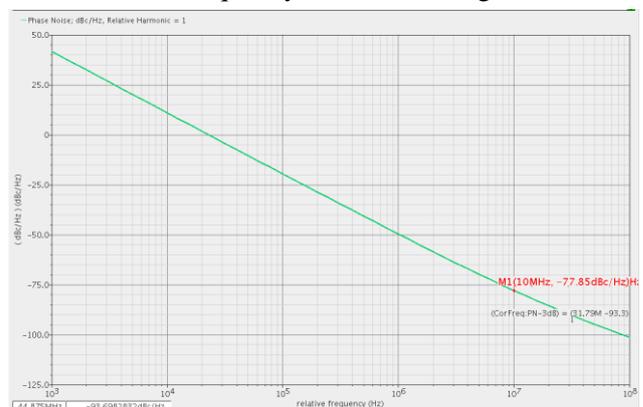


Fig. 6: Phase Noise of the VCRO as a function of offset frequency

#### C. POWER DISSIPATION

At supply voltage  $V_{dd}$  of 1V, the maximum power dissipation of the ring oscillator was found to be 2.9  $\mu$ W which is very small as shown in Fig. 8.



Fig. 7: Power dissipation of ring oscillator

#### IV ANALYSIS OF RESULTS

The performance comparison of various architectures of VCO with different design parameters and technology are mentioned in table II. The frequency range of this VCO is from 6GHz to 17 GHz which is much better than the other works. This wide tuning range of this VCO can be exploited in many applications. The phase noise of this VCO is found to be  $-77.85\text{dBc/Hz}$  @10 MHz offset. This poor phase noise performance is because of the smaller dimension devices which suffer from flicker ( $1/f$ ) noise. The phase noise performance can be improved by increasing the size of the devices used in the delay cell with the cost of more chip area. The power consumption of this VCO is found to be very low as only  $2.97\mu\text{w}$ .

The layout of the circuit is done using cadence tool which is shown in figure

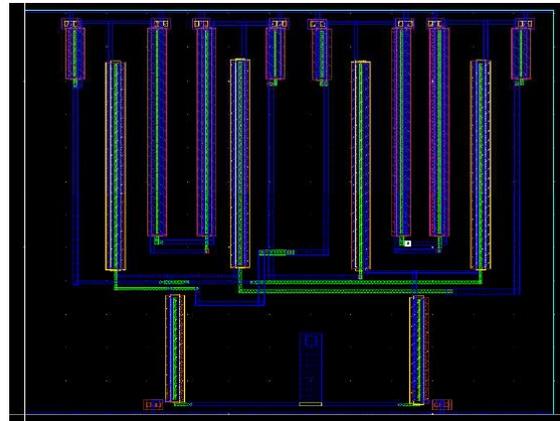


Fig. 8:Layout of the VCO

Table-II: Comparison between different designs of two stage Voltage Controlled Ring Oscillator

Design	Process Technology	Supply(V)	Frequency Range(in MHz)	Power	Phase Noise (dBc/Hz)
W. S. T. Yan and H. C. Luong	0.5 $\mu\text{m}$	2.5	660-1270	15.5 mW	-106 @600KHz offset
Yusuf Jameh Bozorg and Mohammad Jafar Taghizadeh Marvast	65nm	1.2	25GHz	2.49 mW	-137 @ 1 MHz
Aniket Prajapati,P.P.Prajapati	45nm	1	8MHz – 7 GHz	55 $\mu\text{W}$	--
Ghani and Saparon[5]	0.18 $\mu\text{m}$	2	0.7GHz-1.4GHz	14.8mW	-103@600kHz offset
Changzhi Li, and Jenshan Lin	130nm	1.6	1GHz-9GHz	6 mW	-106 @10MHz offset
J.K.Panigrahi and D.P.Acharya [6]	90nm	1.5	1.2GHz-3.2GHz	9.61mW	-90@600kHz offset
This work	45nm	1	6GHz-17GHz	2.9 $\mu\text{W}$	-78 @10MHz offset

#### IV. COMPARISION OF RESULTS

The comparison between different voltage controlled ring oscillators architectures is shown in the table I. From the table, it can be analyzed that the tuning range and power consumption has been

improved up to a great deal. But there is some compromise with the phase noise due to very small size of devices used as smaller devices suffers more flicker noise which is a major constituent of phase noise.

## CONCLUSION

A wide tuning range (6GHz to 17 GHz) and low power consumption (2.9  $\mu$ W at 1 V supply voltage) has been implemented using 45 nm CMOS technology. The phase noise was found to be around -78 dbc/Hz which can be improved by addition of more stages in the oscillator circuit.

## V. REFERENCES

- [1] J. Craninckx and M. Steyaert, "A 1.8-GHz low-phase noise CMOS VCO using optimized hollow spiral inductors," *IEEE J. Solid-State Circuits*, vol. 32, pp. 736–744, May 1997.
- [2] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331–343, Mar. 1996.
- [3] Changzhi Li and Jenshan Lin, "A 1–9 GHz Linear-Wide-Tuning-Range Quadrature Ring Oscillator in 130 nm CMOS for Non-Contact Vital Sign Radar Application," *IEEE Microwave and Wireless Components Letters*, vol. 20, No. 1, Jan. 2010.
- [4] B. Kim and C. H. Park, "A low-noise, 900-MHz VCO in 0.6- $\mu$ m CMOS," *IEEE J. Solid-State Circuits*, vol. 34, pp. 586–591, May 1999.
- [5] Ahmad Akmal Abd Ghani and Azilah Saparon, "A 1.4GHz CMOS Low-Phase Noise Voltage - Controlled Ring Oscillator", The 5th Student Conference on Research and Development – SCORED 2007, 11-12 December 2007, Malaysia.
- [6] D.P.Acharya and J.K.Panigrahi, "Performance Analysis and Design of Wideband CMOS Voltage Controlled Ring Oscillator," International Conference on Industrial and Information Systems, ICIIIS 2010, Jul 29 - Aug 01, 2010.
- [7] Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits," 3<sup>rd</sup> Edition, TATA McGraw-Hill.
- [8] Douglas R. Holberg and Philip E. Allen, "Cmos Analog Design," Oxford.
- [9] B. Razavi, "Design of Analog CMOS integrated circuits," McGraw Hill, 2001.
- [10] Akansha Shrivastava; Saurabh Khandelwal; Shyam Akashe, "Performance Evaluation of Five Stage VCO Ring Oscillator with Reverse Substrate Bias and SAL Technique Using Nanoscale CMOS Technology" 2013 Third International Conference on Advanced Computing and Communication Technologies (ACCT)
- [11] Sajotra Deepak, Dhariwal Sandeep and Mishra Ravi Shankar, "Comparative Analysis of Voltage Controlled Oscillator using CMOS" Indian Journal of Science and Technology, Vol 9(14), DOI: 10.17485/ijst/2016/v9i14/84749, April 2016
- [12] Yusuf Jameh Bozorg and Mohammad Jafar Taghizadeh Marvast , "Designing a new ring oscillator for high performance applications in 65nm cmos technology"
- [13] Aniket Prajapati,P.P.Prajapati, "Analysis of Current Starved Voltage Controlled Oscillator using 45nm CMOS Technology"
- [14] Aman Shivhare, M. K. Gupta, "Low Power Ring Oscillator at 180nm CMOS Technology", International Journal of Computer Applications (0975 – 8887) Volume 144 – No.8, June 2016